

## REMARKS

Applicants respectfully traverse and request reconsideration.

A new ground of rejection was provided in the final action. In the Advisory Action, the Patent Office alleged that the application was not in condition for allowance because the Applicants argued matter “phase lock loop” and “multiple DLLs” on page 10 of the amendment that was not in the claims. However, Applicants respectfully note that claim 9 for example specifically claims a phase shift generating circuit that includes a delay lock loop circuit and that the variable delay circuit includes an input that receives the STROBE signal and is operatively responsive to the delay control signal to provide a phase shifted output signal of the STROBE signal.

In addition, Applicants have added new claim 21 which also sets forth a delay lock loop and other distinguishing features.

Applicants note that in the claims, the signal phase shifting circuit is operative to shift the phase of a STROBE signal based on a clock signal. Foss does not contemplate any type of multiple clock phase circuit such as a feedback delay matching circuit that is coupled to an output of a phase shifting circuit and a signal phase shifting circuit that also employs a variable delay circuit that receives a STROBE signal as claimed.

For example, it appears that the circuit of Foss is more closely related to the clock signal period dividing circuit 22 as known in the prior art. Applicants also respectfully point out that Foss teaches that the output 29 from the multiplexer 27 even when a delay model 33 is employed, activates the enable buffer 8 to output information from memory. As such, as described in Foss, the delay model uses “similar elements as the real circuit path taken by the input clock signal” to compensate for delays for the input clock signal. Foss does not contemplate, teach or suggest the additional compensation or even a need to compensate for delays associated with a receive path of the STROBE signal that already employs an

additional variable delay circuit. As such, the claims are believed to be in condition for allowance.

Stated another way, the Foss reference does not contemplate compensating a clock input and a STROBE input nor compensating for delay variations associated with a phase shifted output signal drive buffer located in a variable delay circuit that receives a STROBE signal as claimed. Accordingly, the independent claims are believed to be allowable for at least these reasons.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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